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EXAMINER	
KUMAR, PANKAJ	

ART UNIT	PAPER NUMBER
2631	7

DATE MAILED: 06/18/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/432,022	Applicant(s) DONOHUE, JOHN E.	
	Examiner Pankaj Kumar	Art Unit 2631	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 February 2003* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-31* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *15-22* is/are allowed.

6)☒ Claim(s) *1-3,7-14 and 23-31* is/are rejected.

7)☒ Claim(s) *4-6* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

Response to Arguments

1. Applicant's arguments filed 2/24/2003 have been fully considered but they are not persuasive.

2. As per constant frequency and interrupted signal, this can occur in a number of ways. Based on paragraphs 5 and 6, interrupted signal is shown in a number of ways such as capacitor can be discharged, voltage difference can be 0, output of VCO can be 0 which would interrupt the input into phase element 60 in fig. 1. Also, fig. 3 shows lines indicating 0 current, or 0 voltage, or L data which are also interrupted signals and these lines during interruption are constant and thus at a constant frequency. Figure 3 also shows such constant lines for different amounts of time which also indicated signal interruption. This is also valid for figure 6.

3. As per Abe teaching decoupling, applicant argues that SW1 is always physically connected to either R1 or R2 and therefore Abe is never decoupling. This argument is respectfully traversed for three reasons.

First, for a momentary time, when SW1 switches, it is not connected to either R1 or R2.

Second, when V1 in fig. 1 does not change as shown in fig. 3, this is equivalent to virtually decoupling since the only reason V1 is still charged (while V1 is constant) is because of the capacitors and not because of the other circuitry. Suppose hypothetically, the circuit left and/or right of V1 is physically decoupled, then V1 will still remain constant. Thus virtually decoupling and physically decoupling produce the same result during this time period.

This same situation is seen in other parts of the circuit. For example, in fig. 3, i2 fluctuates from 0 to some other value. When i2 is 0, this is equivalent to decoupling since if the circuit was physically decoupled, then i2 will still be 0.

Third, R1 can be much larger than R2 (or vice versa) and this is equivalent to decoupling, since if there is a very high resistance, it is like an open circuit. The applicant contests that it is not possible for R1 to be much larger than R2 or vice versa. Abe teaches that R1 and R2 are variables and these variables represent the value of the resistors. Abe has nowhere restricted R1 from being much larger than R2 or vice versa. Abe has not even restricted the values of the variables R1 and R2. Abe inherently teaches that resistors can have any amount of resistance. Accordingly, R1 can be much larger than R2 (or vice versa).

Claim Objections

4. Claim 25 is objected to because of the following informalities: It recites "pair of amplifier input" when it is supposed to be 'pair of amplifier inputs'. Appropriate correction is required.

Claim Rejections - 35 USC § 112

5. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

6. Claims 8-14, 23-31 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

7. Claims 8 and 23 are rejected since 'the input signal' does not specify first, second, or some other input signal.

8. Claims 9-14 are rejected since they depend on claim 8.

9. Claims 24-31 are rejected since they depend on claim 23.

10. Claim 28 recites the limitation "the method of claim 28". There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 102

11. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

12. Claims 1, 2, 3, 8, 10, 14, 23, 24, 26, 30 are rejected under 35 U.S.C. 102(b) as being anticipated by Abe et al. USPN 5319320.

13. As per claim l, Abe teaches a phase locked loop circuit, comprising:

a differential phase detector (Abe fig. 1: 60) that receives an input signal and a feedback signal and produces a differential output signal;

an electronic selector circuit (Abe fig. 1: SW1 with 75 and 70 and possibly other components) having: at least a first input coupled to the differential output of the phase detector (Abe fig.1: via

various components); and ~~with an~~ a second input that is responsive to a detected state of the input signal (Abe fig. 1: responsive by allowing the signal to go through SW1);

a loop filter circuit having an operational amplifier, the operational amplifier ~~based loop filter circuit~~ (Abe fig. 1: 92 and components around it), having at least one amplifier output, wherein the electronic selector circuit provides the differential output signal of the phase detector ~~at a pair of inputs~~ to the ~~operational~~ amplifier input;

a voltage controlled oscillator (Abe fig. 1: 50) coupled to an output of the operational amplifier and providing an output frequency for the phased locked loop circuit; and

wherein the electronic selector circuit is operable to control the ~~input to the operational~~ amplifier input to hold the output frequency of the voltage controlled oscillator at a substantially constant frequency when the input signal to the phase detector is interrupted. (Abe paragraphs 5 and 6: "Since oscillation frequency f.sub.OSC of voltage-controlled oscillator 40 is varied by the value of the filter output voltage V.sub.F, the phase difference between oscillator output V.sub.OUT and input signal S.sub.IN becomes zero as time progresses.

(6) During a time in which signals X.sub.1, X.sub.2 of each period are not generated, an integrated load is stored in capacitor C.sub.F, and, therefore, the output of voltage-controlled oscillator 40 is controlled by that charging voltage. Therefore, the charging voltage of capacitor C.sub.F for current i functions as a frequency control signal for the pull-in operation that matches oscillation frequency f.sub.OSC to the frequency of input signal S.sub.IN."; when the output of VCO is 0, at least one input of the phase comparator, element 60 in fig. 1, is interrupted)

14. As per claim 2, Abe teaches the circuit of claim 1, wherein the electronic selector circuit de-couples the ~~pair of inputs~~ amplifier input from the differential output (if X1 is high and X2 is low then V1 will not change as shown in fig. 3 and thus 60, in fig. 1, is decoupled) and holds the output frequency under an external command when the input signal to the phase detector is interrupted (Abe: see quote above from paragraphs 5 and 6; fig. 1: b1, b2, SW2, 95).

15. As per claim 3, Abe teaches the circuit of claim 2, wherein the electronic selector circuit holds a current signal input to the operational amplifier when a reference signal to the phase detector is interrupted (Abe paragraph 14 "In the above embodiment, filter 75, made from capacitors C.sub.1 and C.sub.2, corresponds to capacitor C.sub.F (see FIG. 4)"; paragraph 6 "During a time in which signals X.sub.1, X.sub.2 of each period are not generated, an integrated load is stored in capacitor C.sub.F, and, therefore, the output of voltage-controlled oscillator 40 is controlled by that charging voltage. Therefore, the charging voltage of capacitor C.sub.F for current i functions as a frequency control signal for the pull-in operation that matches oscillation frequency f.sub.OSC to the frequency of input signal S.sub.IN.").

16. As per claim 8, Abe teaches a phase locked loop circuit, comprising:
a differential phase detector that receives an input signal and a feedback signal and produces a differential output signal (discussed above); an electronic selector circuit having: at least one first input coupled to the differential output of the phase detector; and ~~with an~~ a second input that is responsive to a detected state of the input signal (discussed above; reject with 112 since 'the input signal' does not specify first, second, or some other); a loop filter circuit having an

operational amplifier, the operational amplifier ~~based loop filter circuit,~~ having at least one amplifier input, wherein the electronic selector circuit provides the differential output signal of the phase detector ~~at a pair of inputs~~ to the ~~operational~~ amplifier input (Abe fig. 1: 60 has 2 outputs and 92 has 2 inputs and 60 and 92 are connected via other components); a voltage controlled oscillator coupled to an output of the operational amplifier and providing an output frequency for the phased locked loop circuit; and wherein the electronic selector circuit de-couples the ~~pair of inputs~~ amplifier input from the differential output (Abe in fig. 1 if R1 is much larger than R2 or vice versa, then this equates to decoupling both outputs of the phase detector which are narrowed to just one input into the switch) and holds the output frequency of the voltage controlled oscillator to a last received signal from the differential output when the input signal to the phase detector is interrupted (Abe: paragraphs 5 and 6).

17. As per claim 10, Abe teaches the circuit of claim 8, wherein the amplifier input includes a pair of amplifier inputs and wherein the electronic selector circuit includes a logic based selector circuit which holds the pair of amplifier inputs to an identical potential level to hold the last received signal (Abe fig. 3: V2 is constant at some places) from the differential output at the operational amplifier when the input signal to the phase detector is interrupted (discussed above).

18. As per claim 14, the circuit of claim 8, wherein the output frequency of the voltage controlled oscillator provides the feedback signal to the differential phase detector (Abe fig. 1: output of 50 going to 60).

19. As per claim 23, a method for preventing data errors in a communication system, comprising: coupling input data to a phase locked loop circuit, wherein the phase locked loop includes: a differential phase detector that receives an input signal and a feedback signal and produces a differential output signal; an electronic selector circuit having: at least one first input coupled to ~~a~~ the differential output signal of the phase detector; and a second input ~~with an~~ input that is responsive to a detected state of the input signal (rejected under 112);
a loop filter circuit having an operational amplifier, the operational amplifier ~~based loop filter circuit~~, having at least one amplifier input, wherein the electronic selector circuit provides the differential output signal of the phase detector ~~at a pair of inputs~~ to the ~~operational~~ amplifier input;
and a voltage controlled oscillator coupled to an output of the operational amplifier and providing an output frequency for the phased locked loop circuit; using the electronic selector circuit ~~is operable~~ to control the amplifier input to ~~the operational amplifier~~ to hold the output frequency of the voltage controlled oscillator at a substantially constant frequency when the input signal to the phase detector is interrupted; and using the electronic selector circuit to release control of the ~~input to the operational~~ amplifier input to follow the differential output when the input signal to the phase detector is restored (discussed above).

20. As per claim 24, the method of claim 23, wherein the amplifier input includes a pair of amplifier inputs and wherein using the electronic selector circuit to hold the output frequency of the voltage controlled oscillator at a substantially constant frequency includes using the electronic selector circuit to de-couple the pair of amplifier inputs from the differential output

and hold the output frequency of the voltage controlled oscillator to a last received signal from the differential output when the input signal to the phase detector is interrupted (discussed above).

21. As per claim 26, the method of claim 24, wherein using the electronic selector circuit to decouple the pair of amplifier inputs from the differential output includes using a logic-based selector circuit to hold the pair of amplifier inputs to an identical potential level in order to hold the last received signal from the differential output at the operational amplifier when the input signal to the phase detector is interrupted (discussed above).

22. As per claim 30, the method of claim 23, wherein the method further includes using the output frequency of the voltage controlled oscillator for providing the feedback signal to the differential phase detector (discussed above).

Claim Rejections - 35 USC § 103

23. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

24. Claims 11, 12, 27, 28 rejected under 35 U.S.C. 103(a) as being unpatentable over Abe in view of Satoshi.

25. (103) As per claim 11, Abe teaches the circuit of claim 10. What Abe does not teach are AND gates. What Patent Abstracts of Japan Satoshi Publication number 56,051,140 teaches is wherein the logic based selector circuit includes a pair of AND gates (Satoshi figure AND gates 81, 82), each AND gate having an output coupled to one of the pair of amplifier inputs, wherein one input of each AND gate is coupled to the differential output, and wherein the other input of each AND gate is coupled to an external command signal source. It would have been obvious to one skilled in the art at the time of the invention to modify Abe to include the AND gates in Satoshi as claimed. One would be motivated to do so for the purpose stated in its abstract.

26. As per claim 12, the circuit of claim 11, wherein the external command signal source provides a high potential to one input of each AND gate (Satoshi figure).

27. (103) As per claim 27, the method of claim 26, wherein using a logic-based selector circuit to hold the pair of amplifier inputs to an identical potential level includes using a logic-based selector circuit having a pair of AND gates, coupling an output of each AND gate to one of the pair of amplifier inputs, coupling one input of each AND gate to the differential output, and coupling the other input of each AND gate to an external command signal source. (discussed above)

28. (103) As per claim 28, the method of claim 28, wherein using a logic-based selector having a pair of AND gates and coupling the other input of each AND gate to an external

command signal source includes coupling the other input of each AND gate to a high potential (discussed above).

29. Claim 31 is rejected under 35 U.S.C. 103(a) as being unpatentable over Abe.

30. (103) As per claim 31, Abe teaches the method of claim 23, wherein the method further includes using the output frequency of the voltage controlled oscillator. What Abe does not teach is wherein the method further includes using the output frequency of the voltage controlled oscillator as an output frequency for a system clock coupled to a number of system modules connected to the communication system. It would have been obvious to one skilled in the art at the time of the invention to modify Abe to teach system clock and communication system since it has been held that the selection of known material (in this case, system clock or communication system) based on its suitability for the intended use for prior art parts does not make the claimed invention patentable over that prior art (In re Leshin, 125 USPQ 416). Also, applicant appears compare the method or manner of intended use of the apparatus rather to delineating claimed structure not shown or made obvious by the prior art.

Allowable Subject Matter

31. Claims 15 and 16-22 are allowed.

32. Claims 4, 5 and 6 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

33. Claims 7, 9, 13 and 29 would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 112, second paragraph, set forth in this Office action and to include all of the limitations of the base claim and any intervening claims.

34. Claim 25 would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 112, second paragraph and the objection, both set forth in this Office action and to include all of the limitations of the base claim and any intervening claims.

35. The following is a statement of reasons for the indication of allowable subject matter: The art of record does not suggest the respective claim combinations together and nor would the respective claim combinations be obvious with the bolded portions which are also underlined:

36. Claim 15 is allowed because of ***a number of traffic cards having traffic inputs and traffic outputs***.

37. Claims 16 to 22 are allowed since they depend on claim 15.

38. As per claim 4, the circuit of claim 3, wherein the amplifier input includes a pair of amplifier inputs and wherein the electronic selector circuit holds a current signal input to the operational amplifier by ***coupling the pair of amplifier inputs at the same potential (not in Abe)*** ~~(Abe paragraphs 6 and 14)~~.

39. Claim 5 depends on claim 4

40. As per claim 6, the circuit of claim 2, wherein ***the amplifier input includes a pair of amplifier inputs and wherein the electronic selector circuit includes a logic based selector circuit which holds the pair of amplifier inputs to an identical potential level when the input signal to the phase detector is interrupted (not in Abe)***.

41. As per claim 7, the circuit of claim 2, wherein ***the electronic selector circuit re-couples the ~~pair of inputs~~ amplifier input to the differential output of the phase detector when the input signal is restored (not in Abe)***.

42. As per claim 9, Abe teaches the circuit of claim 8, wherein ***the amplifier input includes a pair of amplifier inputs and wherein the electronic selector circuit includes a switch which couples the pair of amplifier inputs together to hold the last received signal (from the differential output as stated in claim 8) as a current signal input to the operational amplifier when the input signal is interrupted (not in Abe)***.

43. As per claim 13, the circuit of claim 8, wherein ***the electronic selector circuit re-couples the ~~pair of inputs~~ amplifier input to the differential output of the phase detector when the input signal to the phase detector is restored*** (not in Abe).

44. As per claim 25, the method of claim 24, wherein ***using the electronic selector circuit to decouple the pair of amplifier inputs from the differential output includes using a switch to***

couple the pair of amplifier input ~~signals~~ together to hold the last received signal as a current signal input to the operational amplifier when the input signal is interrupted (not in Abe).

45. As per claim 29, the method of claim 23, wherein ***the amplifier input includes a pair of amplifier inputs and wherein using the electronic selector circuit to release control of the ~~input to the operational~~ amplifier input to follow the differential output includes using the electronic selector circuit to re-couple the pair of amplifier inputs to the differential output of the phase detector when the input signal is restored*** (not in Abe).

Conclusion

46. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

47. A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

48. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Pankaj Kumar whose telephone number is (703) 305-0194. The examiner can normally be reached on Monday through Thursday after 8AM to after 6:30PM.

49. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chi H. Pham can be reached on (703) 305-4378. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 872-9314 for regular communications and (703) 872-9314 for After Final communications.

50. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-3800.

PK
June 16, 2003

CHI PHAM
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2600 6/17/03